*A*

***Dissertation on***

**Low Power and Low Leakage Efficient VLSI Design of SRAM Cell Based on 45nm CMOS Technology**

*submitted*

*in partial fulfilment*

*for the award of the Degree of*

***Master of Technology***

***in Department of Electronics & Communication Engineering***

**(with specialization in VLSI & Embedded System Design)**



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April, 2019

***Candidate’s Declaration***

I hereby declare that the work, which is being presented in the Dissertation, entitled **“Low Power and Low Leakage Efficient VLSI Design of SRAM Cell Based on 45nm CMOS Technology”** in partial fulfilment for the award of Degree of “**Master of Technology**” in Deptt. of **Electronics & Communication Engineering** with speciallization in **VLSI & Embedded System Design,** **and submitted to the Department of Electronics & Communication Engineering**, **Apex Institute of Engineering and Technology**, **Jaipur**, Rajasthan Technical University is a record of my own investigations carried under the Guidance of **Mr. Vimal Kr. Agrawal**, Associate Professor, Department of **Electronics & Communication Engineering, Apex Institute of Engineering and Technology**, **Jaipur.**

I have not submitted the matter presented in this Dissertation any where for the award of any other Degree/Diploma.

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**ACKNOWLEDGEMENT**

It’s the foundation of the architecture that defines its ability to stand affirm. The foundation for my research work is just not my sole attempt, but it took efforts and insights of many key people. I sincerely take this opportunity to acknowledge all those who directly or indirectly have been a great support and inspiration throughout the research work.

Firstly, I would like to express my deepest regards to Director Sir, **Prof. O. P. Chhanjani**, Apex Institute of Engineering and Technology, who has the attitude and the substance of a genius: he continually and convincingly conveyed a spirit and excitement in research.

Now I would like to address one of my key mentors: **Mr. Vimal Kr. Agrawal,** Associate Professor, Apex Institute of Engineering and Technology, Jaipur. It has been an honour to be his research student. He consciously or unconsciously leveraged his key and creative insights wherever applicable in the research work. Amidst of his busy schedule, he made himself available for any query related to work almost every time. I sincerely appreciate his contribution in terms of time and ideas. I would also like to acknowledge all of my supportive and encouraging colleagues who made a significant contribution during each phase of dissertation directly or indirectly.

Lastly I would like to thank my parents, my family and friends for their love, motivation and encouragement in my all pursuits. Last but not the least my special thanks go to my institute, **Apex Institute of Engineering and Technology, Jaipur** for giving me this opportunity to work in the great environment.

With sincere thanks from

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**ABSTRACT**

The explosive growth of battery operated devices has made low-power design a priority in recent years. Moreover, embedded SRAM units have become an important block in modern Silicon on Chips. The increasing number of transistor count in the SRAM units and the surging leakage current of the MOS transistors in the scaled technologies have made the SRAM unit a power hungry block from both dynamic and static perspectives. Owing to high bitline voltage swing during write operation, the write power consumption is dominated the dynamic power consumption. The static power consumption is mainly due to the leakage current associated with the SRAM cells distributed in the array. Moreover, as supply voltage decreases to tackle the power consumption, the data stability of the SRAM cells have become a major concern in recent years.

To reduce the write power consumption, several schemes such as row based sense amplifying cell (SAC) and hierarchical bitline sense amplification (HBLSA) have been proposed. However, these schemes impose architectural limitations on the design in terms of the number of words on a row. Beside, the effectiveness of these methods is limited to the dynamic power consumption. Conventionally, reduction of the cell supply voltage and exploiting the body effect has been suggested to reduce the cell leakage current. However, variation of the supply voltage of the cell associates with a higher dynamic power consumption and reduced cell data stability.

In this thesis efficient low power design of 4 transistors SRAM cell is analyzed. Performance of the design is verified by using 130nm and 45nm UMC CMOS technology. Design is simulated in HSPICE tool for the successful function of the SRAM cell. Performance of the design is measured in terms of average power consumption. Design is simulated for different values of resistance and capacitance. According to that average power is calculated. Optimized values of resistance and capacitance are taken.

**Chapter 1**

**INTRODUCTION**

Developments in embedded memory technology have made large Dynamic Random Access Memories (DRAMs) and Static Random Access Memories (SRAMs) common place in today's System on Chips (SoCs.) Tradeoffs between large and small memories have made all sizes practical, enabling SoCs to resemble board-level systems more than ever. Large embedded memories give a SoC a number of benefits such as improved bandwidth and considerable performance that can only be achieved through the use of embedded technologies. The possibility and success of including embedded DRAM and/or large SRAM blocks in a SoC depends mainly on manufacturability.

Embedded SRAMs are the prominent embedded memories used in today's SoCs. SRAM's integrability with standard CMOS technology gives it an ample opportunity to become the highest area consumer of many SoCs ranging from a high performance server processor to a an HDTV video processor SRAMs do not require data refreshing mechanism. This is because an SRAM cell can store the data indefinitely as long as it is powered. This feature saves the complex and the area consuming data refreshing periphery circuits and makes medium size SRAM units a feasible choice for implementation in the standard CMOS process [1].

**1.1 Introduction**

With the advancement in technology, digital circuits play a very important role. Digital circuits are less susceptible to noise or degradation in quality than analog circuits. It is also easier to perform error detection and correction with digital signals. A computer system, either it be a large machine or be a microcomputer, needs memory for storing data and program instructions. In a computer system there are various types of memories using a variety of technologies and having different access times. The main memory is generally the most easily obtained memory. It is the one from which all instructions in programs are executed. The main memory is generally of the random-access type. A random-access memory (RAM) is defined as the memory in which the time required for storing/writing and accessing/reading data is independent of the location in which the information is stored. The read-write (R/W) memory circuits are designed to allow the change (writing) of data bits to be stored in the memory array, as well as their access (reading) on demand. The memory circuit is said to be static if the stored data can be retained indefinitely without any need for a periodic refresh operation as long as the suitable power supply is provided. To a great extent static random access memory is used in superior performance processors as catches. Cache memory is the fastest memory in a computer. SRAMs alone possess a large area in the processor and as a result contribute an important part of total power dissipation of the system. Different SRAM topologies are 4T, 5T, 6T, 7T, 8T, 9T, etc. The performances of the SRAM cells are evaluated on the basis of its performance index comprising of parameters like, stability, power, delay, etc. The stability of the cell is measured through Static Noise Margin [2] (SNM) which is obtained from the butterfly curves. Another method for the performance evaluation is the Noise-curves method, popularly known as the N-curves.

Continuous scaling of the MOS devices has resulted to a tremendous improvement in the performance of MOS devices at the cost of increased threshold voltage, leakage current variation, short channel effects, reduced gate control, severe process variation and unmanageable power densities. This scaling has progressed rapidly for three decades, but may soon come to an end. Therefore, alternative technologies to bulk silicon transistors are being explored. A minimum sized SRAM cell is highly needed for increasing the memory integration density. As the integration of components increases, leakage power becomes a prime concern in today’s memory chips. Lower voltages and smaller devices cause a significant degradation of data stability in cells. So the development of a memory technology with greater stability and lower power consumption characteristics is, highly desirable.

**1.2 Memory Array**

Memory arrays often account for the majority of transistors in a CMOS system-on-chip. Arrays may be divided into categories as shown in Fig. 1.1. Random access memory is accessed with an address and has latency independent of the address. In contrast, serial access memories are accessed sequentially so no address is necessary. Content addressable memories determine which address (es) contain data that matches a specified key. Random access memory is commonly classified as read-only memory (ROM) or read/write memory (confusingly called RAM). Even the term ROM is misleading because many ROMs can be written as well. A more useful classification is volatile vs. nonvolatile memory. Volatile memory retains its data as long as power is applied, while nonvolatile memory will hold data indefinitely. RAM is synonymous with volatile memory, while ROM is synonymous with nonvolatile memory.

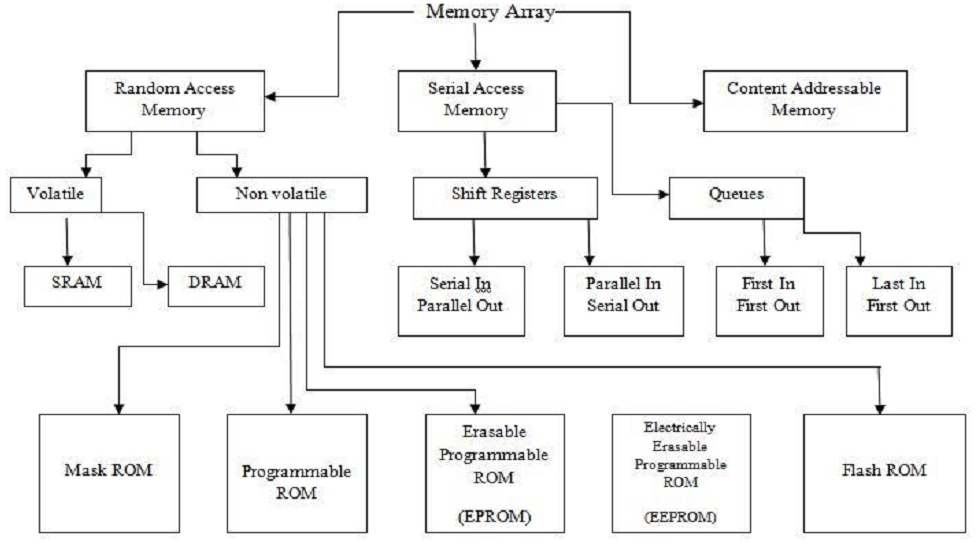


Fig. 1.1 Memory array

Like sequencing elements, the memory cells used in volatile memories can further be divided into static structures and dynamic structures. Static cells use some form of feedback to maintain their state, while dynamic cells use charge stored on a floating capacitor through an access transistor. Static RAMs (SRAMs) are faster and less troublesome, but require more area per bit than their dynamic counterparts (DRAMs).

A memory array contains 2n words of 2m bits each. Each bit is stored in a memory cell.

Fig. 1.2 shows the memory array architecture. The row decoder uses the address to activate one of the rows by asserting the word line. During a read operation, the cells on this word line drive the bit lines, which may have been conditioned to a known value in advance of the memory access [3]. The column circuitry may contain amplifiers or buffers to sense the data. A typical memory array may have thousands or millions of words of only 8–64 bits each, which would lead to a tall, skinny layout that is hard to fit in the chip floor plan and slow because of the long vertical wires. Therefore, the array is often folded into fewer rows of more columns.

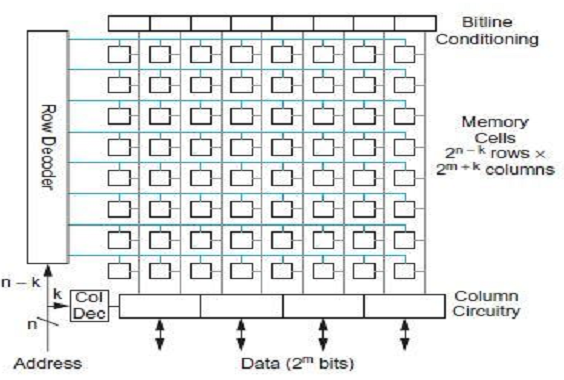


Fig. 1.2 Memory array structure

After folding, each row of the memory contains 2k words, so the array is physically organized as 2 n–k rows of 2 m+k columns or bits. Fig. 1.2 shows a two-way fold (k = 1) with eight rows and eight columns. The column decoder controls a multiplexer in the column circuitry to select 2m bits from the row as the data to access. Larger memories are generally built from multiple smaller sub arrays so that the word lines and bit lines remain reasonably short, fast, and low in power dissipation.

**1.3 Application of SRAM**

The integrability of embedded SRAMs have made it a prominent choice for the digital signal processors (DSPs) that operate along with the over-sampling analog to digital (A/D) and digital to analog (D/A) data converters. Over-sampling data converters are the most popular choices for the low-power applications where the accuracy of the conversion is a demanding requirement.

Amplitude and phase/frequency domain over-sampling data converters has been widely used in the wireless communication systems. These types of data converters are based on the noise shaping property of a closed loop system. Hence, the accuracy of the conversion is being traded off by sampling rate of the data converter. This feature makes the sampling frequency to be several times that of the Nyquist frequency of the signal bandwidth. In return, the accuracy of the samples is relaxed [4, 5].

In the over-sampling data converters the quantization noise is shaped such that the noise is pushed out of the signal band width after its being digitized using a filter. After the signal is being digitized, it needs to be down-sampled (decimated) to the Nyquist frequency of the signal bandwidth. In order to avoid aliasing in the down-sampling process, out of band noise needs to be suppressed. This purpose is served by decimation filters.

In many cases, decimation filters are usually implemented as finite impulse response (FIR) filters or infinite impulse response (IIR) filters in a DSP [6]. This makes the DSP an inseparable part of an over-sampling data conversion front-ends. In many cases the DSP is designed such that it also performs other signal processing as well as coding/decoding which is demanded in a monolithic receiver. This consideration shares the resources on the chip and reduces the overall cost and power consumption.

The DSP requires a memory to store its temporary data. For example, to implement a decimation filter, each filter tap takes a certain memory location in an embedded memory. This requirement makes a memory block a key component in an integrated receiver (Fig. 1.3). It is noteworthy that SRAMs are widely used in many other applications such as cache memories of multi-purpose processors.

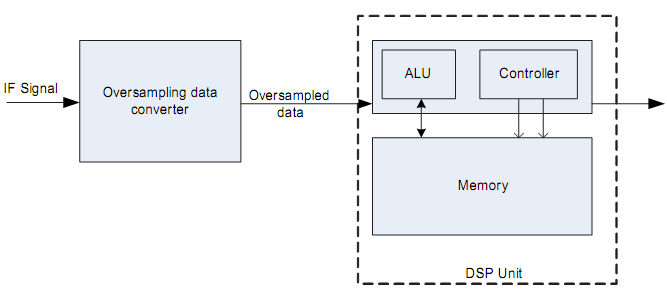


Fig. 1.3 Role of memory in receiver

SRAM is more expensive and less dense than DRAM and is therefore not used for high-capacity, low-cost applications such as the main [memory](https://en.wikipedia.org/wiki/Computer_memory) in [personal computers](https://en.wikipedia.org/wiki/Personal_computer). The [power](https://en.wikipedia.org/wiki/Electric_power) consumption of SRAM varies widely depending on how frequently it is accessed; it can be as power-hungry as dynamic RAM, when used at high frequencies, and some [ICs](https://en.wikipedia.org/wiki/Integrated_circuit) can consume many [watts](https://en.wikipedia.org/wiki/Watt) at full bandwidth. On the other hand, static RAM used at a somewhat slower pace, such as in applications with moderately clocked microprocessors, draws very little power and can have a nearly negligible power consumption when sitting idle – in the region of a few micro-watts. Several techniques have been proposed to manage power consumption of SRAM-based memory structures. SRAM is used

* As RAM or cache memory in micro-controllers.
* As the primary caches in powerful microprocessors, such as the [x86](https://en.wikipedia.org/wiki/X86) family, and many others (from 8 [KB](https://en.wikipedia.org/wiki/Kilobyte), up to many megabytes).
* To store the registers and parts of the state-machines utilized in some microprocessors.
* In application specific IC, or [ASIC](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit).
* In [FPGA](https://en.wikipedia.org/wiki/FPGA) and [CPLD](https://en.wikipedia.org/wiki/CPLD).
* In many categories of industrial and scientific subsystems, automotive electronics, and similar.
* In practically all modern appliances, toys, etc. that implement an electronic user interface.
* In complex products such as digital cameras, cell phones, synthesizers, etc.
* In personal computers, workstations, routers and peripheral equipment: CPU [register files](https://en.wikipedia.org/wiki/Register_file), internal [CPU caches](https://en.wikipedia.org/wiki/CPU_cache) and external [burst mode](https://en.wikipedia.org/wiki/Burst_mode_(computing)) SRAM caches, [hard disk](https://en.wikipedia.org/wiki/Hard_disk) buffers, [router](https://en.wikipedia.org/wiki/Router_(computing)) buffers, etc.

[LCD screens](https://en.wikipedia.org/wiki/LCD_screen) and [printers](https://en.wikipedia.org/wiki/Computer_printer) also normally employ static RAM to hold the image displayed (or to be printed). Static RAM was used for the main memory of some early personal computers such as the [TRS-80 Model 100](https://en.wikipedia.org/wiki/TRS-80_Model_100) and [Commodore VIC-20](https://en.wikipedia.org/wiki/Commodore_VIC-20).

**1.4 Motivation**

Over the past few years, with the explosive growth of battery operated devices such as wireless communication units, portable multi-media devices, and implantable bio-medical chips the demand for low-power integrated circuits has been significantly increased. According to International Technology Roadmap for Semiconductors (ITRS)-2003 [7], SRAM is going to take more than 60% of the SoCs in a near future. As the technology scales, the density of the transistors in the SRAM units increases substantially. Fig. 1.4 shows the trend of the transistor density according to [8]. This figure suggests that the majority of the transistors on a chip are going to sit in the SRAM unit.

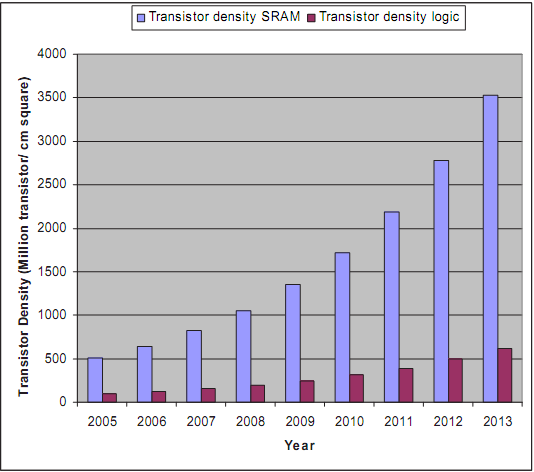


Fig. 1.4 Transistor density trends

Leakage current issue is especially important since it loses the low-power advantage of the CMOS circuits that we take for granted today. As the technology scales, the leakage current increases by several orders of magnitude. According to [9], the leakage current is the highest contributor to the standby power consumption of the Intel Pentium processors and there is an ongoing effort to restrain this current through device enhancement and circuit techniques. The high subthreshold leakage current has conventionally been dealt with to keep the overall leakage current within tolerable limits for high-performance chips. One common approach is to fabricate more than one type of transistor on the chip, including the high-performance, low threshold voltage device described above, as well as other transistors(s) with a higher threshold voltage and larger area to reduce the leakage current. The high-performance device is used just in critical paths, and the low leakage devices are used everywhere else. This approach, however, has achieved limited success for the medium size embedded SRAM units because of the area overhead of the high-Vth transistors and the extra cost of the dual Vth process [10].

In addition to the static power consumption, the dynamic power consumption of the SRAM units is becoming an issue as the technology scales. This is particularly important on high density blocks where heavily capacitively loaded interconnects are located. As the technology scales, the distance between the metal layers becomes shorter. Consequently, the capacitance of the interconnects increases thus influencing the dynamic power consumption. This concern becomes especially important in high density blocks such as SRAM units where the interconnects are at their minimum distance from each other and are loaded with the capacitive load of a plurality of cells.

The reduction of the supply voltage is the most effective way in reducing both dynamic and static power consumption. Reduction of the supply voltage of the SRAM cells is known to have an adverse effect on the data stability of the SRAM cells. These cells are already under data stability problems as the technology scales.

**1.5 Problem Statement**

The aim of this work is to minimize the average power consumed by SRAM cell. Two efficient designs of 6 transistor SRAM cell and 4 transistor SRAM cell are analyzed with suitable transistor characteristics and executed by applying 130nm UMC CMOS technology The optimized design should be such that it consumes less power, give high duty cycle so that it can be implemented in high speed optical communication systems. Average power consumption is calculated for both the designs.

**1.6** **Thesis Organization**

This thesis includes five Chapters which are mentioned as follows:

**Chapter 1: INTRODUCTION.** This chapter includes basic introduction of SRAM, memory array and architecture, applications of SRAM. It also includes motivation of work, objective of our research and organization of this thesis.

**Chapter 2:** **LITERATURE REVIEW**. This chapter defines the work performed by many researchers in the field of enhancing the SRAM cell features.

**Chapter 3:** **BASICS OF SRAM**. This chapter initially defines basic definition of SRAM. Then it defines different categories of SRAM. It also includes detailed description of operation of SRAM cell. Then it defines some performance parameters of SRAM, architecture of SRAM cell array. Lastly it defines some configurations of SRAM cell.

**Chapter 4: POWER CONSUMPTION IN SRAM.** This chapter defines static and dynamic power consumption in SRAM. It also defines power minimization techniques.

**Chapter 5: INTRODUCTION TO HSPICE TOOL.** This chapter defines basic introduction of HSpice tool, its operation and its advantages. It also defines process of simulation in HSpice. Then it includes basic introduction of CosmosScope waveform editor. Lastly it defines the technology nodes used in program simulation.

**Chapter 6: PROPOSED WORK.** This chapter includes design of 4T SRAM cell, its transistor characteristics and simulation results for read and write operation. Comparison table in terms of average power consumption is also included in it. Design is simulated for different values of resistance and capacitance. According to that average power is calculated.

**Chapter 7:** **CONCLUSION AND FUTURE SCOPE**. This chapter includes summary of the project and comparison between previous and proposed design in terms of average power consumed. It also includes the work which can be done further.

**Chapter 2**

**LITERATURE REVIEW**

Memory is used widely in all electrical systems: mainframes, microcomputers and cellular phones, etc. The growing demand of portable battery operated systems has made energy efficient processors a necessity. The performance of these devices is limited by the size, weight and lifetime of batteries. Serious reliability problems, increased design costs and battery-operated applications prompted the IC design community to look more aggressively for new approaches and methodologies that produce more power-efficient designs, which means significant reductions in power consumption for the same level of performance. Memory circuits form an integral part of every system design as Dynamic RAMs, Static RAMs, Ferroelectric RAMs, ROMs or Flash Memories, significantly contributing to the system level power consumption. Reducing the power dissipation in memories can significantly improve the system power-efficiency, performance, reliability and overall costs. RAMs have experienced a very rapid development of low-power low-voltage memory design during recent years due to an increased demand for notebooks, laptops, hand-held communication devices and IC memory cards.

There are various approaches that are adopted to reduce power dissipation, like design of circuits with power supply voltage scaling, power gating and drowsy method. Lower power supply voltage reduces the dynamic power in quadratic fashion and leakage power in exponential way. But power supply voltage scaling results in reduced noise margin. Many SRAM arrays are based on minimizing the active capacitance and reducing the swing voltage. In sub-100nm region leakage currents are mainly due to gate leakage and sub threshold leakage current. High dielectric constant gate technology decreases the gate leakage current. Forward body biasing methods and dual Vt techniques are used to reduce sub threshold leakage current. In sub threshold SRAMs power supply voltage (VDD) is lower than the transistor threshold voltage (Vt) and the sub threshold leakage current is the operating current.

**Seevinck, 1987 [11]:** The stability of both resistor-load (R-load) and full-CMOS SRAM cells is investigated analytically as well as by simulation. Explicit analytic expressions for the static-noise margin (SNM) as a function of device parameters and supply voltage are derived. The expressions are useful in predicting the effect of parameter changes on the stability as well as in optimizing the design of SRAM cells. An easy-to-use SNM simulation method is presented, the results of which are in good agreement with the results predicted by the analytic SNM expressions. It is further concluded that full-CMOS cells are much more stable than R-load cells at a low supply voltage.

**Itoh, 1995 [12]:** Trends in low-power circuit technologies of CMOS RAM chips are reviewed in terms of three key issues: charging capacitance, operating voltage, and dc current. The discussion includes a general description of power sources in a RAM chip, and covers both DRAM’s and SRAM’s. In DRAM’s, successive circuit advancements have produced a power reduction equivalent to two to three orders of magnitude over the last decade for a fixed memory capacity chip. Coupled with the low-power advantage of CMOS circuits, two technologies have been the major contributors to power reduction: lower charging capacitance due to partial activation of multi-divided arrays that use multi-divisions of data and word lines and lower operating voltage resulting from external power supply reduction, half-VDD pre-charging, and on-chip voltage down converting scheme. In SRAM’s, partial activation of a multi-divided word line drastically reduces the dc current from the data-line load to the selected cell. In addition to advances in the sense amplifier circuit, an auto power down scheme that uses address transition detection for word driver and column circuitry further reduces the dc current. It is also shown that to design ultralow voltage DRAM’s and SRAM’s, the application of sub threshold current reduction circuits (such as source-gate back biasing) to cell and iterative circuit blocks will be indispensable in the future.

**Ivanger et al. 2004 [13]**: They have given a description of an embedded high density 128Kb SRAM memory using 5 Transistors single bit line memory cell in standard 0.18µm CMOS technology. Switching the bitline to either ‘Vcc’ or ‘Vss’, writing of ‘1’ or ‘0’into a 5 Transistor cell has been execuited, whereas the wordline is kept at Vcc. As a result, for a proper read operation, the bit line is precharged to an average voltage level Vpc=600mV which is less than 1.8V. The 128Kb memory that is based on the 5 Transistors SRAM cell has 23% lesser area, 75% smaller bitline leakage, and a write/read performance similar to a conventional 6 Transistor cell.

**Cheng and Huang, 2005 [14]:** This paper presents a low-power SRAM design with quiet-bitline architecture by incorporating two major techniques. Firstly, the authors use a one-side driving scheme for the write operation to prevent the excessive full-swing charging on the bitlines. Secondly, they use a precharge free pulling scheme for the read operation so as to keep all bitlines at low voltages at all times. SPICE simulation on a 2K-bit SRAM macro shows that such architecture can lead to a significant 84.4% power reduction over a self-designed baseline low-power SRAM macro.

**Ming, 2005 [15]:** This paper describes a low-power write scheme by adopting charge sharing technique. By reducing the bitlines voltage swing, the bitlines dynamic power is reduced. The

memory cell's static noise margin (SNM) is discussed to prove it is a feasible scheme. Simulation results show compare to conventional SRAM, in write cycle this SRAM saves more than 20% dynamic power.

[**Ramy E. Aly**](http://ieeexplore.ieee.org/search/searchresult.jsp?searchWithin=%22Authors%22:.QT.Ramy%20E.%20Aly.QT.&newsearch=true) **et.al, 2007 [16]:**On-chip cache consumes a large percentage of the whole chip area and expected to increase in advanced technologies. Charging/discharging large bit lines capacitance represents a large portion of power consumption during a write operation. We propose a novel write mechanism which depends only on one of the two bit lines to perform a write operation. Therefore, the proposed 7T SRAM cell reduces the activity factor of discharging the bit line pair to perform a write operation. Experimental results using HSPICE simulation shows that the write power saving is at least 49%. Both read delay and static noise margin are maintained after carefully sizing the cell transistors.

**Athe and Gupta, 2009 [17]:** Data retention and leakage current reduction are among the major area of concern in today’s CMOS technology. In this paper 6T, 8T and 9T SRAM cell have been compared on the basis of read noise margin (RNM), write noise margin (WNM), read delay, write delay, data retention voltage (DRV), layout and parasitic capacitance. Corner and statistical simulation of the noise margin has been carried out to analyze the effect of intrinsic parameter fluctuations. Both 8T SRAM cell and 9T SRAM cell provides higher read noise margin (around 4 times increase in RNM) as compared to 6T SRAM cell. Although the size of 9T SRAM cell is around 1.35 times higher than that of the 8T SRAM cell but it provides higher write stability. Due to single ended bit line sensing the write stability of 8T SRAM cell is greatly affected. The 8T SRAM cell provides a write “1” noise margin which is approximately 3 times smaller than that of the 9T SRAM cell. The data retention voltage for 8T SRAM cell was found to be 93.64mV while for 9T SRAM cell it was 84.5mV and for 6T SRAM cell it was 252.3mV. Read delay for 9T SRAM cell is 98.85ps while for 6T SRAM cell it is 72.82ps and for 8T SRAM cell it is 77.72ps. The higher read delay for 9T SRAM cell is attributed to the fact that dual threshold voltage technology has been in it in order to reduce the leakage current. Write delay for 9T SRAM cell was found to be 10ps, 45.47ps for 8T SRAM cell and 8.97ps for 6T SRAM cell. The simulation has been carried out on 90nm CMOS technology.

**G. M., Sreerama Reddy et. Al, 2009 [18]:** They presented a design and analyzed 8Mb Static Random Access Memory (SRAM) at 90nm, focusing on optimizing power and delay. The SRAM access path is split into two portions: from address input to word line rise (the row decoder) and from word line rise to data output (the read data path). Techniques to optimize both of these paths are investigated and implemented. In this work the existing SRAM architectures are investigated, and then a basic 6T SRAM structure was chosen. The decoder, excluding the predecoder, which constitutes the path from address input to the word line rise, is implemented as a binary structure by implementing a multi-stage path. For fast lower power solutions, the heuristic of reducing the sizes of the input stage in the higher levels of the decode tree allows for good trade-offs between delay and power. The key to low power operation in the SRAM data path is to reduce the signal swings on the high capacitance nodes like the bit lines and the data lines. While designing the SRAM, techniques such as circuit partitioning, gate oxide thickness variations and low power layout techniques are made use of to minimize the power dissipation. The mask design of the constituent memory blocks is done using virtuoso tool, the DRC & LVS verified through Hercules/Calibre and finally, the characterization is done on single bit SRAM cell to determine the cell characteristics (mainly power) in static as well as dynamic modes. The results obtained after performing the characterization of a single bit SRAM cell are presented in this paper.

**W. Mann et. al., 2010 [19]:** Large scale 6T SRAM beyond 65 nm will increasingly rely on assist methods to overcome the functional limitations associated with scaling and the inherent read stability/write margin trade off. The primary focus of the circuit assist methods has been

improved read or write margin with less attention given to the implications for performance. In this work, they introduce margin sensitivity and margin/delay analysis tools for assessing the functional effectiveness of the bias based assist methods and show the direct implications on voltage sensitive yield. A margin/delay analysis of bias based circuit assist methods is presented, highlighting the assist impact on the functional metrics, margin and performance. A means of categorizing the assist methods is developed to provide a first order understanding of the underlying mechanisms. The analysis spans four generations of low power technologies to show the trends and long term effectiveness of the circuit assist techniques in future low power bulk technologies.

**Yen Hsiang Tseng et al., 2010 [20]**: They have shown that the conventional 4T and 6T SRAM cells endured from external noise, as they have a direct path belonging to the storage nodes and the bit line. Here a 7T SRAM cell is proposed that does not have any direct path belonging to the bit line and the storage node, therefore has higher endurance towards external noise. In the proposed work the cell consists of separate data access mechanism for read and write operations. The circuits are implemented by TSMC 1-Poly 6-Metals 0.1-um CMOS process. Simulation results indicate the read SNM enhanced by 1.6X and 0.31X compared to 4T and 6T.

**Mohammad, 2011 [21]:** Leakage power becomes big percentage of total active power especially for small geometry CMOS technology. It is estimated that 20-50% of total average power during normal operation lost to leakage power. Leakage power is even more important for mobile devices where ideal time is long and battery life is important. This paper presents a low leakage SRAM cell and array architecture targeting high performance, low power embedded memory. The proposed novel 7-Transistor (7T) based memory provides 50% lower leakage power compare to 8T cell and 30% faster access time than traditional 6-Transistor (6T) SRAM cell with increased area of20% compared to the compact 6T cell. All comparisons are based on 28nm foundry low power process technology.

**Karimi and Alimoradi, 2011 [22]:** Rapid growth in semiconductor technology has led to shrinking of feature sizes of transistors using deep submicron (DSM) process. As MOS transistors enter deep submicron sizes, undesirable consequences regarding power consumption arise. Until recently, dynamic or switching power component dominated the total power dissipated by an IC. Voltage scaling is perhaps the most effective method to decrease dynamic power due to the square law dependency of digital circuit active power on the supply voltage. As a result, this demands a reduction of threshold voltage to maintain performance. Low threshold voltage results in an exponential increase in the sub-threshold leakage current. On the other hand as technology scales down, shorter channel lengths result in increased sub-threshold leakage current through an off transistor. Therefore, in DSM process static or leakage power becomes a considerable proportion of the total power dissipation. For these reasons, static power consumption, i.e. leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies.

**Hussain and Jahinuzzaman, 2012 [23]:** In this work, a gated ground SRAM architecture based on a seven transistor (7T) bit-cell is proposed. The proposed cell shows higher data stability and yield under varying process, voltage, and temperature (PVT) conditions than the conventional 6T cell. A single-ended sense amplifier is also presented to read from the proposed cell while a unique write mechanism is used to reduce the write power to less than half of the write power of the 6T cell. The proposed cell consumes similar silicon area and leakage power as the 6T cell when laid out and simulated using a commercial 65-nm CMOS technology. The ground gating is done by selectively controlling the column virtual ground (CVG) of accessed word in a row. This significantly reduces the leakage power consumption and enables implementing multiple words per row, which lowers multiple-bit data upset in the event of radiation induced single event upset or soft error. In addition, the proposed cell inherently has a 30% larger soft error critical charge, making its soft error rate (SER) less than the half of that of the 6T cell.

**Zhu and Kursun, 2014 [24]:** Conventional Static Random Access Memory (SRAM) cells suffer from an intrinsic data instability problem due to directly-accessed data storage nodes during a read operation. Noise margins of memory cells further shrink with increasing variability and decreasing power supply voltage in scaled CMOS technologies. A seven-transistor (7T), an eight-transistor (8T), a nine-transistor (9T), and 3 conventional six-transistor (6T) memory circuits are characterized for layout area, data stability, write voltage margin, data access speed, active power consumption, idle mode leakage currents, and minimum power supply voltage in this paper. A comprehensive electrical performance metric is evaluated to compare the memory cells considering process parameter and supply voltage fluctuations. The triple-threshold-voltage 8T and 9T SRAM cells provide up to 2.5x stronger data stability and 765.9x higher overall electrical quality as compared to the traditional 6T SRAM cells in a TSMC 65 nm CMOS technology.

**Mitra, 2014 [25]:** Speed, power consumption and area, are some of the most important factors of concern in modern day memory design. As we move towards Deep Sub-Micron Technologies, the problems of leakage current, noise and cell stability due to physical parameter variation becomes more pronounced. In this paper we have designed an 8T Read Decoupled Dual Port SRAM Cell with Dual Threshold Voltage and characterized it in terms of read and write delay, read and write noise margins, Data Retention Voltage and Leakage Current. Read Decoupling improves the Read Noise Margin and static power dissipation is reduced by using Dual-Vt transistors. The results obtained are compared with existing 6T, 8T, 9T SRAM Cells, which shows the superiority of the proposed design. The Cell is designed and simulated in TSPICE using 90nm CMOS process.

**Hemant Bansal et al, 2015 [26]:** They analyzed the 6-transistors SRAM memory cell at 90 nm and 180nm CMOS technologies by using the Tanner tool which is having a supply voltage of 1.8 volts. Simulation results indicate that 1-bit 6T SRAM memory cell has lesser average power consumption and power-delay product as compared to the conventional SRAM cell at 90nm and 180nm technologies. So it can be used as today’s VLSI design technology. There is also an improvement in the delay in case of newly designed 1-bit 6T SRAM memory cell at 180nm technology as compared to the conventional SRAM cell but in case of 1-bit 6T SRAM memory cell at 90nm it takes more time in comparison to that in the conventional SRAM cell. In case of 64-bits 6T SRAM memory cell, there is lesser average power consumption, propagation delay and power-delay product at 90nm technology as compare to 64-bits 6T SRAM memory cell at 180nm technology.

**Soumitra et al. 2015 [27]:** They have designed noise tolerant and lower power consumption stable differential SRAM cell. The proposed work is similar to 6T SRAM cell with addition of two buffer transistors, a complimentary bit line and a tail transistor. Stacking effect enables lower power dissipation in the proposed cell. Effects of process parameter variations, such as threshold voltage, length on Read Static Noise Margin (RSNM), read access (TRA), write access time (TWA) is also presented. The proposed work obtains improvements in TWA and read/write/hold power consumption in comparison to 6T cell. Simulation results are obtained in 16nm PTM technology and verified using TSMC 180nm technology.

**Nitish Nagpal et.al, 2016 [28]:**Theypresented a paper for power consumption which is a main concern these days for long operational life. Although numerous types of techniques to decrease the power dissipation has been developed. One of the most adopted method is to lower the supply voltage In this paper static random access memory parameters like low power, high performance circuit and characteristics and applications.

**Jaspreet Kaur et.al, 2016 [29]:** They presented a paper for continuous scaling of the transistor size and reduction of the operating voltage has led to a significant performance improvement of integrated circuits. Low power consumption and smaller area are the most important criteria for the fabrication of DSP systems. Static random access memories (SRAMs) consist of almost 90% of very large scale integrated (VLSI) circuits. The ever-increasing demand for larger data storage capacity has driven the fabrication technology and memory development toward more compact design rules and, consequently, toward higher storage densities. This paper deals with design of low power static random-access memory (RAM) cells and peripheral circuits for standalone RAMs, in 32nm focusing on stable operation and reduced leakage power dissipation. The work is carried out on Tanner Tool version 13 at 32nm technology.

**T. Vishnupriya et.al, 2017 [30]**: They presented a new method of incorporating adiabatic logic like use of adiabatic switch and ECRL in conventional SRAM cell designs. These proposed designs have reduced power and noise compared to conventional design and thus the proposed designs are further implemented in latest nano-devices. Simulations are carried out using Tanner EDA Tool and HSPICE Synopsis.

**Chapter 3**

**BASICS OF SRAM**

Memory cells are the key components of any SRAM unit. An SRAM cell can store one bit of data. An SRAM cell comprises two back-to-back connected inverters forming a latch and two access transistors. Access transistors serve for read and write access to the cell. SRAMs are widely used in applications from caches to register files to tables to scratchpad buffers. The SRAM consists of an array of memory cells along with the row and column circuitry. An SRAM cell offers the following basic properties:

* Retention: An SRAM cell is able to retain the data indefinitely as long as it is powered.
* Read: An SRAM cell is able to communicate its data.
* Write: The data of an SRAM cell can be set to any binary value regardless of its original data.

A number of SRAM cell topologies have been reported in the past decade. Among these topologies, resistive load four-transistor (4T) cell, loadless 4T cell and six transistor (6T) SRAM cell have received attention in practice, owing to their symmetry in storing logic `one' and logic `zero'. [1]. The data retention in the 4T SRAM cells is ensured by the leakage current of the access transistors.

**3.1 Categories of SRAM**

Different types of SRAM can be described according to different categories. These categories are as follows:

* **Data retention**
* **Non-volatile SRAMs:** They have standard SRAM functionality, but they save the data when the power supply is lost, ensuring preservation of critical information. They are used in a wide range of situations—networking, aerospace, and medical, among many others where the preservation of data is critical and where batteries are impractical.
* **Volatile SRAMs:** They are also used to store data but don’t save the data. Data is erased when the power supply is lost.
* **Transistor type**
* [**Bipolar junction transistor**](https://en.wikipedia.org/wiki/Bipolar_junction_transistor) **SRAM**: It is used in [TTL](https://en.wikipedia.org/wiki/Transistor-transistor_logic) and [ECL](https://en.wikipedia.org/wiki/Emitter_coupled_logic) and very fast but consumes a lot of power.
* [**MOSFET**](https://en.wikipedia.org/wiki/MOSFET) **SRAM**: It is used in [CMOS](https://en.wikipedia.org/wiki/CMOS). It consumes low power and very common today.
* **Function type**
* [**Asynchronous**](https://en.wikipedia.org/wiki/Asynchronous) **SRAM**: It is independent of clock frequency; data in and data out are controlled by address transition. In 1990s asynchronous SRAM memory used to be employed for fast access time. Asynchronous SRAM was used as [main memory](https://en.wikipedia.org/wiki/Main_memory) for small cache-less embedded processors used in everything from [industrial electronics](https://en.wikipedia.org/wiki/Industrial_electronics) and [measurement systems](https://en.wikipedia.org/wiki/Measurement_system) to [hard disks](https://en.wikipedia.org/wiki/Hard_disk) and networking equipment, among many other applications [31].
* [**Synchronous**](https://en.wikipedia.org/wiki/Synchronization) **SRAM**: In this SRAM all timings are initiated by the clock edge(s). Address, data in and other control signals are associated with the clock signals. Synchronous memory interface is much faster as access time can be significantly reduced by employing [pipeline](https://en.wikipedia.org/wiki/Pipeline_(computing)) architecture. SRAM memory is much faster for random access. Therefore SRAM memory is mainly used for [CPU cache](https://en.wikipedia.org/wiki/CPU_cache), small on-chip memory, [FIFOs](https://en.wikipedia.org/wiki/FIFO_(computing_and_electronics)) or others buffers.
* **Feature**
* [**ZBT**](https://en.wikipedia.org/w/index.php?title=Zero_bus_turnaround&action=edit&redlink=1)**(zero**[**bus turnaround**](https://en.wikipedia.org/w/index.php?title=Bus_turnaround&action=edit&redlink=1)**) SRAM**: The turnaround is the number of clock cycles it takes to change access to the SRAM from write to read and vice versa. The turnarounds for ZBT SRAMs or the latency between read and write cycle is zero.
* [**Sync-Burst**](https://en.wikipedia.org/w/index.php?title=SyncBurst&action=edit&redlink=1)**(synchronous-burst) SRAM**: It features synchronous burst write access to the SRAM to increase write operation to the SRAM.
* [**DDR SRAM**](https://en.wikipedia.org/w/index.php?title=DDR_SRAM&action=edit&redlink=1): Synchronous, single read/write port, double data rate I/O.
* [**Quad Data Rate SRAM**](https://en.wikipedia.org/wiki/Quad_Data_Rate_SRAM)**:** Synchronous, separate read and write ports, quadruple data rate I/O.
* **Flip-flop type**
* **Binary SRAM:** Binary logic gates are used to store 0 & 1.
* **Ternary SRAM:** Ternary logic gates are used to store ternary values i.e. 2 (for high), 1 (for medium) and 0 (for low). Compared to binary logic, ternary logic allows more information to be transmitted over a given set of lines thus reducing the chip area.

**3.2 Operation of SRAM Cell**

Single bit 6 transistor SRAM memory cell is shown in Fig. 3.1.

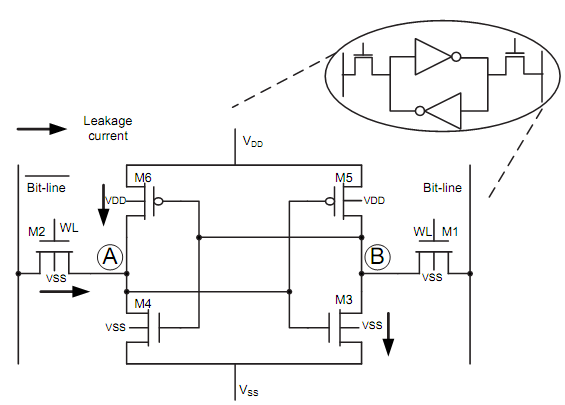


Fig. 3.1 6T SRAM cell schematic

A SRAM cell needs to be able to read and write data and to hold the data as long as the power is applied. An ordinary flip-flop could accomplish this requirement, but the size is quite large. The 6T SRAM cell shown in Fig. 3.1 achieves its compactness at the expense of more complex peripheral circuitry for reading and writing the cells [17].

The small cell size offers shorter wires hence lower dynamic power consumption. The central challenges in SRAM design are minimizing its size and ensuring that the circuitry holding the state is weak enough to be overpowered during a write, yet strong enough not to be disturbed during a read.

A 6T SRAM cell consists of two cross-coupled CMOS inverters and two access transistors. The output (input) of the inverters construct the internal nodes of the cell. Once active, the access transistors facilitate the communication of the cell internal nodes with the input/output ports of the cell. The input/output ports of the cell are called bitlines (BL and BL.) Bitlines are a shared data communications medium among the cells on the same column in an array of cells. Consequently, they have high capacitive loading. The read and write operations are conducted through the bitlines.

**3.2.1 Read Operation**

Fig. 3.2 (b) illustrates the operation of the cell during a read access.

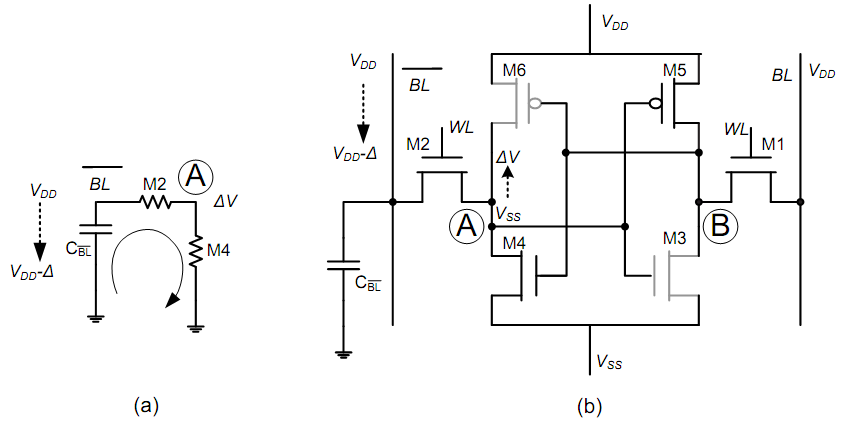


Fig. 3.2 Read operation of SRAM cell (a) Discharging of bitline (b) equivalent circuit during read operation

In this figure, node A carries a logic `zero' and node B carries a logic `one' before the cell is accessed. Thus, the gray transistors, M3 and M6, are `off' while M4 and M5 are 'on' and compensate for the leakage current of M3 and M6. In conventional design, the bitlines are precharged to VDD before the read operation begins.

Activation of the wordlines (WL), i.e., the gate of the access transistors, initiates the read operation. As the wordline goes high, M2 goes to saturation region while M4 operates in triode region. Owing to the short-channel effect, the current associated with M2 has a linear relationship with the voltage of the node `A' [1]. Hence, these transistors behave like a resistor in this operation. Therefore, M2 and M4 form a voltage divider and raise node `A' voltage by ΔV. This voltage drives the input of the inverter M5-M3. To ensure a non-destructive read operation ΔV is chosen such that it does not trigger the M5-M3 inverter and node B remains at VDD over the entire cell access time. Having a constant voltage of VDD at the gate of M4 warrants the constant resistivity assumption for M4 over the access time.

Fig. 3.2 (a) shows the linear model of the bitline discharge path. In this model the bitline capacitance of CBLbar is precharged to VDD. Upon the activation of M2, CBLbar discharges through M2 and M4 and causes a voltage drop of Δ on BLbar. Since the gate source voltage of M1 remains at zero volts (i.e., Vgs1 = 0V), CBL cannot discharge and remains at VDD. The differential voltage between BL and BLbar, Δ, is amplified using a sense amplifier to produce the regular logic levels. Clearly, a faster bitline discharge can be achieved by reducing the resistance in the discharge path. However, such improvements come at the price of larger cell transistor sizes which is not recommended for high density SRAMs.

Waveform for read ‘1’ operation is shown in Fig. 3.3.

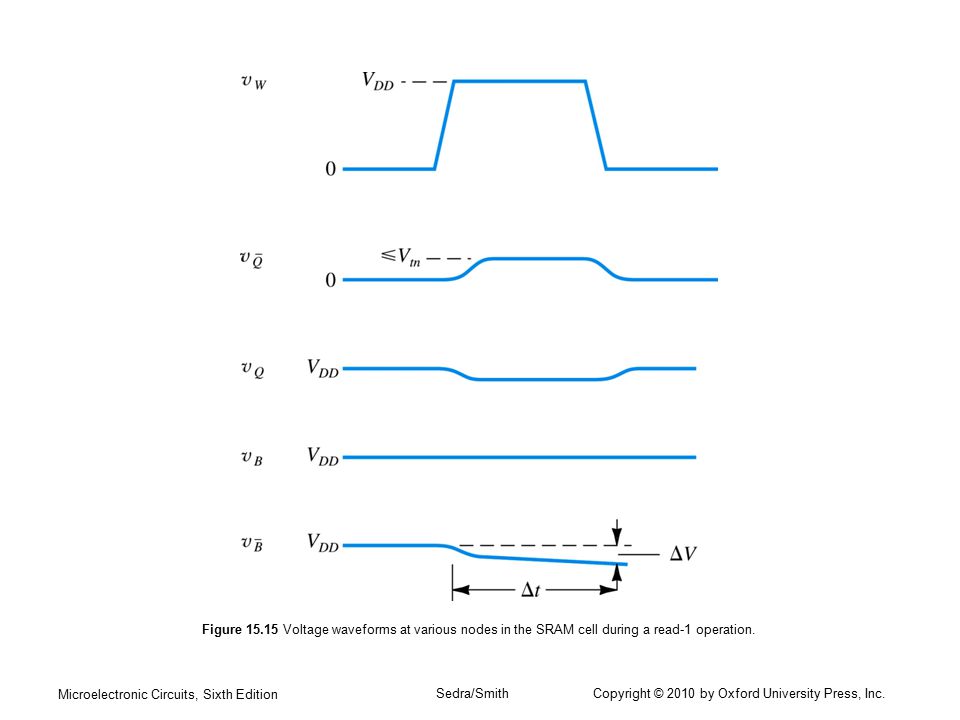


Fig. 3.3 Waveform for read ‘1’ operation

In fig. 3.3 we can see that initially bitline and bitlinebar are precharged to VDD. When wordline is high bitline voltage remains constant but bitlinebar voltage decreases due to discharging. This discharging results in increase in Qbar voltage. It states that output at Q is high (1).

**3.2.2 Write Operation**

Fig. 3.4 (a) illustrates the operation of the cell in the write operation.

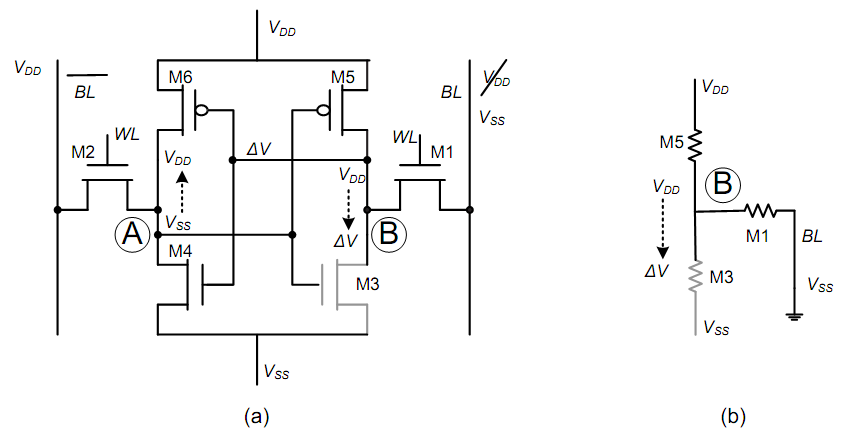


Fig. 3.4 Write operation of SRAM cell (a) Discharging of bitline (b) equivalent circuit during write operation

In this figure the initial conditions of nodes A and B are VSS and VDD, respectively. Re-writing the old data to the cell is trivial so we concentrate on changing the data of the cell. In other words, the write operation is complete only if the voltage level on node A and B become VDD and VSS, respectively.

The activation of the wordline can not cause a sufficient voltage increase on node A to trigger the inverter M5-M3 if both bitlines are precharged to VDD. Therefore, the write operation is conducted by reducing the bitline associated with node B, BL, to a sufficiently low voltage (e.g., VSS.) This operation forms a voltage divider comprising of M5 and M1 at the beginning of the operation. A sufficiently low ΔV triggers the inverter M6-M4 which results in charging up node A to VDD. Since node A drives the inverter M5-M3, node B is pulled down to VSS through M3 and M5 turns off. Hence, the logic state of the cell is changed. The wordline becomes inactive after the completion of the operation.

Waveform for write operation is shown in Fig. 3.5.

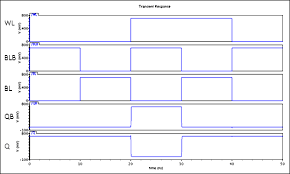


Fig. 3.5 Waveform for write operation

In fig. 3.5 we can see that initially value of Q is 1. When wordline is high bitline voltage goes low and bitlinebar voltage goes high. This condition will write ‘0’ in SRAM cell. Then bitline voltage goes high and bitlinebar voltage goes low. This condition will write ‘1’ in SRAM cell.

**3.3 Performance Parameters of SRAM**

**Static Noise Margin** abbreviated as SNM is defined as the measure of stability of the SRAM cell to hold its data against noise. SNM of SRAM is defined as minimum amount of noise voltage present on the storing nodes of SRAM required to flip the state of cell. SNM can be computed as the length of the side of a maximum square nested between the two voltage transfer characteristic (VTC) curves (i.e., for each back to back inverters) of SRAM cell. SNM can be categorized as Hold SNM and Read SNM. Hold SNM is the SNM of the cell when word line is LOW or disabled, meaning that the cell is in standby mode. However, the read SNM is more critical than the hold SNM because the SRAM is more vulnerable during read operation when word line is active [32].

**Write Static Noise Margin** briefed as WSNM is the measure of the ability to write data into the SRAM cell. In a write operation, two operations take place. Firstly discharging of node storing ‘1’ and pull up transistor PMOS and access transistor NMOS are responsible for the discharging of the node ‘1’. Secondly charging of node ‘0’ through pull up transistor PMOS. Write margin voltage is the maximum noise voltage present on bit lines during successful write operation.

**Static Current Noise Margin** abbreviated as SINM is defined as the maximum value of the DC current that can be introduced in the SRAM cell before its content changes. It is given by the peak value of Iin during read operation.

**Write Trip Voltage** is the information regarding the write ability of the cell is provided by the N-curves. The WTV is the voltage drop needed to flip the internal node “1” of the cell with both the bit lines clamped to supply (Vdd).

**Write Trip Current** is the amount of current needed to write the cell when both bit lines are clamped at supply (Vdd). The peak value of Iin after the second zero crossing of N-curve gives WTI.

**Write power** is the dynamic power defined as, the power dissipated by a memory cell during write operation. The write power dissipation is higher due to the full swing charge and discharge on the bitlines during write operation.

**Write delay** is defined as the time taken by the SRAM cell to write data into the cell or the time taken by the cell to flip its contents. It is calculated by performing transient analysis in the write operation.

**Read delay** is the delay involved in allowing the bit lines to discharge by about 10% of the peak value or the delay between the application of the WL signal and the response time of the sense amplifier.

**Leakage power** is the power consumed by a device not related to state changes (also referred to as static power). Leakage power is actually consumed when a device is both static and switching, but generally the main concern with leakage power is when the device is in its inactive state, as all the power consumed in this state is considered “wasted” power.

**3.4 Transistor Sizing**

The W/L ratio of the transistor is selected to provide the gate with current driving capability in both the directions equal to that of the basic inverter. From the basic inverter design (W/L)n is usually 1.5 to 2 and for a matched design, (W/L)p=(µn/µp)(W/L)n. The SRAM cell must be designed such a way that, during read operation, the changes in Q and Qbar are small enough to prevent the cell from changing its state. Generally two back to back coupled inverters of the SRAM cell is designed so that Kn and Kp are matched [33]. This design places the inverter threshold at VDD/2. The size of the access transistors are usually made 2 to 3 times wider than Kn of the inverters. To achieve optimum operation of the cell following (W/L) ratio is choose for different transistors. A minimum ratio of 2 is required for NMOS transistors of inverters and 4 is necessary for PMOS transistors. Access transistors must be made double wider or more by providing a W/L ratio of more than 4. But these set of ratios does not match with the design rule of Cadence Virtuoso layout editor for 0.18 micron technology. For 0.18 µ technology minimum width for an NMOS transistor comes out to be 0.6 µ. Thus (W/L) ratio is 3.33. For PMOS transistor the ratio becomes 6.66. This implies a width of 1.2 µ. Based on the SPICE simulation results and its analysis, W/L ratio for access transistor is kept at 9.99. This refers to a gate width of 1.8 µ.

**3.5 Architecture of SRAM Unit**

The periphery blocks in an SRAM unit facilitate access to the cells for the read or write operation. In practice, multiple bits are accessed for the read or write operation at the same time. The group of bits that are accessed at the same time form a word. Depending on application, the word size, M, usually varies from a dozen bits to 64 bits. In regular SRAMs only one word is accessed at a time. The number of words that are accommodated in the unit specifies the length of address field, N. However, The total number of cells in an array can be calculated as M x N.

An SRAM unit consists of several periphery blocks. An array accommodates the plurality of cells. A decoder decodes the binary encoded input address to indicate the physical location of the addressed cell(or word.) Sense amplifiers (SA) and write drivers interface with the bitlines to communicate with the cell in read and write operations, respectively. A timing control unit generates the proper timing signals for the activation of the wordline, SA or write driver during the read or write operation, respectively.

A plurality of cells organized beside each other form an array. The cells sitting on the same row share the same wordline. Cells on the same column share the same pair of bitlines. Fig. 3.6 illustrates the construction of an array and the associated bitlines and wordlines. Clearly, the numerous cells on the same bitline and the short distance between the neighboring columns impose a significant capacitive load on the bitlines. For every access, only one wordline is active in an array. Activation of the wordline causes all SRAM cells on the row to discharge their corresponding bitlines. Hence, all the bitlines are discharged as a result of wordline activation.

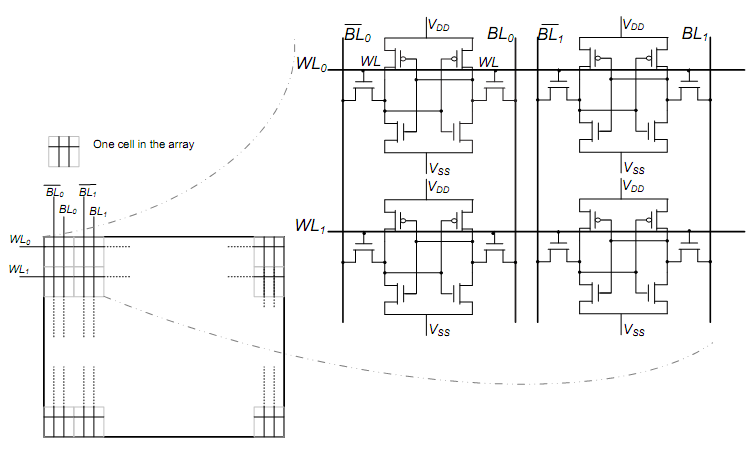


Fig. 3.6 SRAM cell array

Number of cells in each column can be extended to 128 or more than that depending on the specification of the SRAM. The SRAM circuit can be extended to 128x8 block memory. This can be accomplished by adding additional SRAM cells in each column. Total 128 SRAM cells can be added in a column. These cells are addressed by a 7x128 row decoder. The outputs of row decoder from R0 to R127 are connected to word lines of individual row SRAM cells. All WL of each row SRAM cells are tied together. Thus with the help of total 10 address bits we can address whole 128x8 block of 210=1024 bits. To make simulation process and analysis simple, only one row and 8 columns (i.e. total 8 SRAM cells) is constructed. Once it is proved that this cell array works as expected then the same concept can be extended for higher size of SRAM.

**3.6 Different Configurations of SRAM Cell**

Various configurations of SRAM cell are used in different devices. Each configuration has some advantages and disadvantages. Operation of some configuration is as follows:

**3.6.1 4T SRAM Cell**

Four Transistor SRAM cells holds a very significant position in the SRAM market since, they occupy much less area than other greater number of transistors SRAM cell. Fig. 3.7 shows CMOS SRAMs, the cells comprise of two PMOS driver transistors and two NMOS pass transistors to access the cell. The bit lines BL and BLB are precharged to ground instead of VDD.

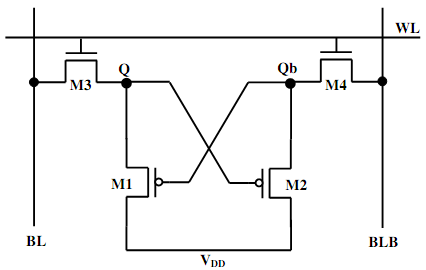


Fig. 3.7 4T SRAM cell

**Write operation:** To store logic “0” to the cell BLB is charged to VDD and BL is charged to ground and vice versa for storing a “1”. Now the word line is switched to VDD to turn on the NMOS access transistors [34]. As soon as the word line is turned on the bit line value is written into the Q and QB of the cell. After the completion of the write operation the word line voltage is reset to ground level to turn the NMOS off.

**Read operation:** The read operation of the 4T cell is different from the 6T cell. To read the cell the bit lines are precharged to ground instead of VDD and the word line to VDD to turn on NMOS access transistors. Node storing a high value will pull the bit line to a higher value. The other bit line is pulled to ground.

**Standby operation:** In the standby mode, the cell remains in idle state. The wordline WL is not asserted and so the access transistors remain off. And the two cross-coupled PMOS continuously reinforce each other to hold the stored data.

**3.6.2 5T SRAM Cell**

Five transistors SRAM cell shown in Fig. 3.8 has single bit line and only one access transistor.

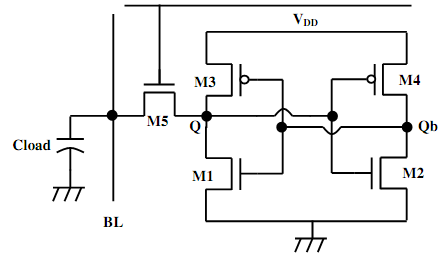


Fig. 3.8 5T SRAM cell

**Write operation:** Writing a ‘0’ or a ‘1’ into the cell is performed by driving the single bit line BL to VDD or ground (where VDD is the supply, i.e. 0.9V) and the word line is also asserted to Vcc. The write ability is ascertained by different cell sizing strategy. As a result this circuit provides smaller bit line leakage, lesser area compared to conventional 6T cell.

**Read operation:** For a non-destructive read operation the bit line is precharged to an intermediate voltage Vpc = 300mV which is less than 0.9V supply.

**3.6.3 7T SRAM Cell**

The seven transistors SRAM cell relies on cutting off the feedback between the two inverters, inv1 and inv2, before a write operation [20]. The feedback connection and disconnection is maintained through an extra NMOS transistor as shown in Fig. 3.9 and in order to perform a write operation the cell depends only on BLbar.

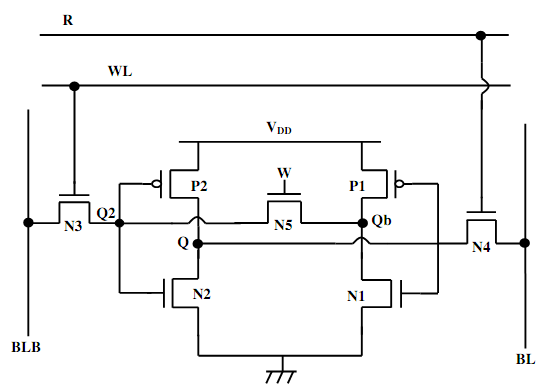


Fig. 3.9 7T SRAM cell

**Write operation:** The write operation begins by turning N5 off in order to cut off the feedback. BLbar contains complement of the input data, N3 is turned on, while N4 is kept off. After the feedback disconnection the 7T SRAM cell looks like two cascaded inverters, inv2 followed by inv1. N3 passes the data from BLbar to Q2 which drives inv2, P2 and N2, to develop Q, the cell data. Similarly, Q drives inv1, P1 and N1, to obtain Qbar which equals Q2 if data is “0” and slightly higher than Q2 if data is “1”. Then, WL is turned off and N5 is turned on to reconnect the feedback link between the two inverters to stably store the new data. To store the value “1” in the cell, BLbar is discharged to “0” with similar power consumption to the conventional 6T cell. To store a “0” in the cell, there is no need to discharge BLbar and therefore, the activity factor of discharging BLbar is less than 1 and depends on the percentage of writing “1.”

**Read operation:** Both WL and R signals are turned on, while N5 is kept on. When Q=”0”, the read path consists of N2 and N4, and behaves like a conventional 6T cell. When Q=”1”, the read path consists of N1, N5 and N3, which represents a critical read path. In this critical side, the three transistors are connected in series which reduces the driving capability of the cell unless these transistors are carefully sized.

**Chapter 4**

**POWER CONSUMPTION IN SRAM**

Identification of different components that contribute to the power consumption of an SRAM unit is critical to minimize the overall power consumption. The power consumption of the SRAM unit can be divided into two major terms; static and dynamic.

Static power consumption is the amount of power that is consumed by the unit to retain the data. Unlike many passive memory devices, an SRAM cell needs to be powered to keep the data. Although the amount of power that a cell consumes to retain the data is relatively small, when a plurality of cells is implemented, the total static power consumption can become significant. Static power consumption can be a major source of power consumption especially in large, low frequency SRAMs as well as SRAMs in scaled down technologies. The static power is also referred to as leakage power in digital circuit design since the static power consumption is due to the leakage current passing through the circuit when there is no activity.

Dynamic power consumption of the SRAM unit is especially important when the speed of operation is high. The long interconnects with high capacitive loading require a significant amount of charge for their voltage variation. Owing to the interconnect's regular pattern and predictable switching activity factor, ®, the power consumption associated with the interconnects that undergo a full swing voltage variation can be accurately calculated using the famous dynamic power consumption equation [1]:

where f is the frequency of operation, Cinterconnect is the interconnect capacitance and Vdd is the supply voltage.

**4.1 Static Power Consumption**

The static power consumption in an SRAM unit is mainly due to the leakage current in SRAM cells. If several blocks are used, then the leakage current of the AND gates in the local row-decoders can become significant. However, for sufficiently large row sizes (e.g., more than 32-bits) the leakage current of the post decoders can be neglected compared to the leakage current of the SRAM cells.

According to [35], among different leakage current mechanisms, the subthreshold leakage of the off transistors are the prominent source of the leakage current in an SRAM cell. The next important leakage current in the SRAM cells for currently available technologies is the gate induces drain leakage (GIDL) which is usually more than one order of magnitude smaller than the subthreshold leakage in the 130nm CMOS technology. Fig. 4.1 shows different components of the leakage current in an SRAM cell when the cell is in the non-accessed mode (i.e., access transistors are off).

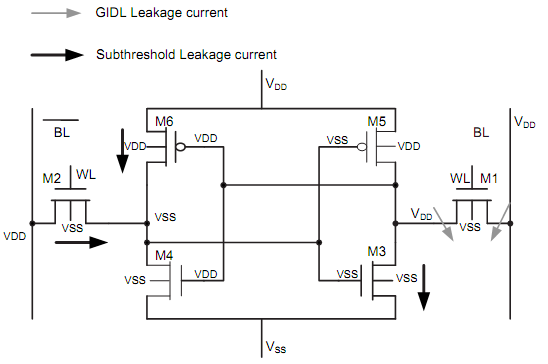


Fig. 4.1 Leakage current when SRAM cell is not operating

The leakage current associated with the transistors that are off (i.e., M1, M2, M3 and M6) constitutes the total leakage current. The gate source voltage, Vgs of the transistors M3 and M6 are equal to zero because of the nature of the cross coupled loop. However, the subthreshold current of the access transistor M2 depends on the wordline voltage. Owing to a negative Vgs, the subthreshold leakage current of the transistor M1 is substantially smaller compared to the GIDL associated with that transistor. However, as long as the gate voltage does not go below the substrate voltage, the GIDL current associated with M1 is negligible in comparison to the subthreshold leakage currents of the other off transistors.

**4.2 Dynamic Power Consumption**

The read and write dynamic power consumption of an SRAM unit can be calculated by adding up the dynamic power consumption associated with different capacitive loads that is charged and discharged during the read and write operation, respectively. Clearly, the total dynamic power consumption is mainly dominated by the long interconnects which impose a large capacitive load to the signal paths in the SRAM unit. For example, the outputs of the pre-decoders at the row decoder which are loaded by the post decoder, block decoder's output, the wordlines and bitlines and the column decoder's output are considered as heavily loaded interconnects.

To simplify the calculations, the energy consumption associated with different nodes can be calculated, separately. Let's assume that a block comprises of R rows and L = M x 2n columns, where M is the word size and 2n is the number of words on the same row. The dynamic energy consumption associated with each capacitor during the read and write operation can be calculated provided that the voltage variation of these capacitors is known.

Bitline voltage variation of VDD during the write operation constitutes a prominent fraction of the dynamic energy consumed by the SRAM unit. This fact has compelled many designers to combat the write power consumption by reducing the bitline capacitance [36] or by reducing the bitline discharge voltage [37] in recent years.

**4.3 Power Consumption Minimization Techniques**

* **Clock gating:** The disconnecting of the clock from a device it drives when the data going into the device is not changing. This technique is used to minimize dynamic power [21].

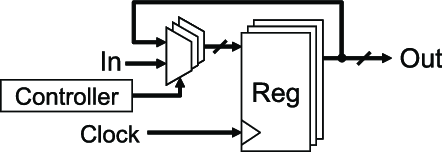


Fig. 4.2 Clock gating

* **Multi-Vth optimization**: The replacement of faster Low-Vth cells, which consume more leakage power, with slower High-Vth cells, which consume less leakage power. Since the High-Vth cells are slower, this swapping only occurs on timing paths that have positive slack and thus can be allowed to slow down( Fig. 4.3 [22]).

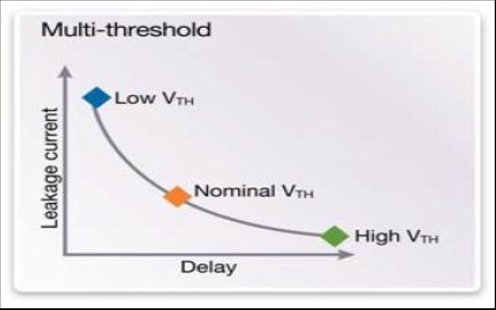


Fig. 4.3 Multi-Vth optimization

As technologies have shrunk, leakage power consumption has grown exponentially, thus requiring more aggressive power reduction techniques to be used. Similarly, clock frequency increases have caused dynamic power consumption of the devices to outstrip the capacity of the power networks that supply them, and this becomes especially acute when high power consumption occurs in very small geometries, as this is a power density issue as well as a power consumption issue.

* **Multi supply voltage**: Multiple voltage rails (multi-Vdd) can be supplied to a design to impact power and performance. A higher voltage yields a faster the circuit, but with higher the dynamic power. In many designs, only discrete portions of the design need to run at high speed. Other portions may only operate at lower speeds, and thus require lower voltages therefore consume less power [22].

**Chapter 5**

**INTRODUCTION TO HSPICE TOOL**

HSPICE is just a programming tool that takes netlist (a general text file comprising a circuit description and analysis options) as an input and generates the analysis it has executed on the circuit as output. An HSPICE netlist generally has an .sp extension, for example circuit.sp. Although HSPICE generates various output files, the only file that we require to investigate for the research work is the file which has .lis extension, for example circuit.lis. This file includes all of the important simulation results from the analysis such as operating points, measurement results, error messages, etc. Commonly after simulating a circuit, it is better to examine this file initially to assure there were no errors in our netlist.

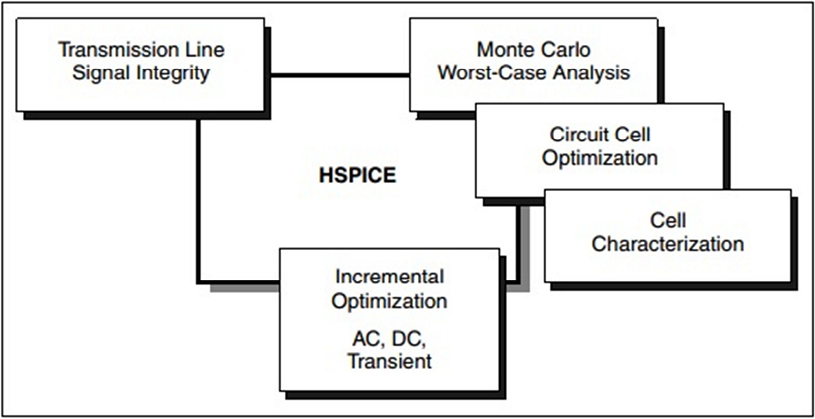


Fig. 5.1 Design features of HSpice

As seen in Fig. 5.1 HSPICE form the base of a set of Synopsys tools and services that allows accurate calibration of logic and circuit model libraries to actual silicon performance. The memory acts as a limiting factor to the size of the circuits simulated by HSPICE. It is a 32-bit application and can address 2Gb or 4Gb of memory at the maximum [38].

HSpice Circuit Simulator keeps you in control of simulation works with an easy-to-use graphical interface and a faster, more advanced design atmosphere. Having key features like multi- device state plotting, threading support, real-time waveform viewing and analysis, and a command window for creation of simpler SPICE syntax, HSpice consumes less time and money during the simulation stage of our design flow. HSpice allows more accurate simulations by supporting the advanced models of transistor such as BSIM4 and the Penn State Philips (PSP) model. Specified that HSpice is compatible with a broad range of design solutions and executes on Windows and Linux platforms, it adjusts easily and cost effectively into your present design flow.

As shown in Fig. 5.2, HSPICE performs various types of simulation experiments like single point, sweep, etc. followed by initial condition description, circuit, analysis, results etc.

Different analysis lie DC, AC and Transient.

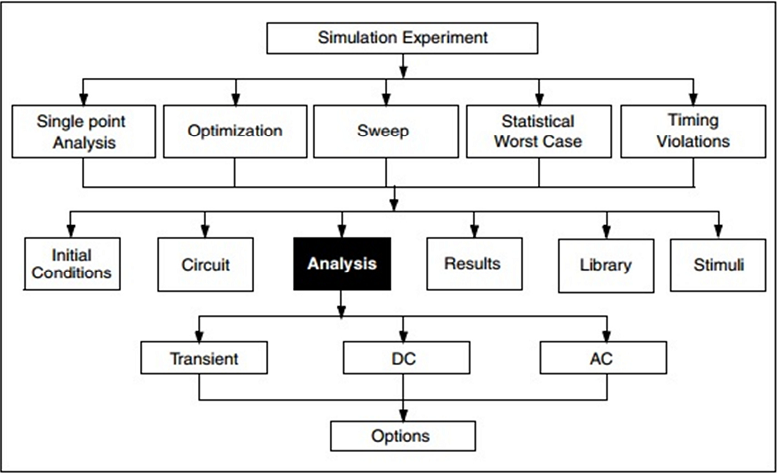


Fig. 5.2 Simulation structure of HSpice

CosmosScope is an analyzer tool for graphical waveform that enables us to view and examine simulation results in the form of waveforms represented on graphs, or as values represented in lists. Tools associated with CosmosScope are:

* Signal Manager: With the help of this tool, the plotfiles are opened, filtered, and represented in a graph window or calculator.
* Measurement Tool: It gives more than 50 types of measurements that can be implemented to a waveform.
* Waveform Calculator: It includes a hand-held calculator that communicates graphically with the application.
* Command Line Tool: It enables us to enter AIM commands, write scripts, and save them into files.

**5.1 Advantages of HSpice**

* **Speed:** HSpice gives highly optimized programming code for computing device models, formulating the functions of linear equations, and solving those functions. Moreover the standard direct model assessment, HSpice also gives the option of table-base transistor model assessment, in which the simulation results of device model evaluations are kept stored in tables and reutilized. Because assessment of device models may be computationally expensive, this method can produce dramatic simulation speed enhances [38].
* **Convergence:** HSpice utilizes advanced mathematical techniques to obtain superior numerical stability. Very large circuits and feedback circuits, not possible to analyze with other SPICE tools, can be simulated in HSpice tool.
* **Accuracy:** HSpice utilizes very accurate numerical techniques and charge conservation to obtain superior simulation accuracy.
* **Input language extensions:** HSpice input language is an advanced version of the standard SPICE language. It includes much advancement, consisting of parameters, algebraic expressions and a powerful bit and bus input wave specification syntax.
* **Runtime waveform viewing:** The Cosmos scope waveform analyzer displays graphical results during simulation. Analysis in HSpice results in form of currents, voltages, charges and power may be written to single or multiple files.
* It supports gate and body resistance circuits in RF modeling process.
* Executes non-quasi-static (NQS) modeling process.
* Supports complete geometry-based parasitic device models for multi-finger devices.
* Supports self-heating and RF resistor circuits.
* Enables easy generation of syntax-correct SPICE with the help of a command wizard.
* Provides Accurate, Fast and Precise options to allow optimal balance of performance and accuracy.
* DC and AC analysis can be executed.
* Advanced noise analysis can be executed.
* Monte Carlo analysis over unlimited variables and trials with device and lot of variations.

**5.2 Flow of Process**

The mechanism below defines an HSPICE simulation and an analysis procedure in CosmosScope tool.

* Initially start Notepad. We can perform this either by clicking Start → Run, typing “Notepad”, and pressing Enter. Or, we can go for Start → Programs → Accessories → Notepad.
* Copy the sample text in Notepad exactly as it is specified (this is known as “netlist”).

SPICE Tutorial Example 1 - General RC Circuit

vs vs gnd PULSE(0V 1V 5ms 5.001ms 10ms 20ms)

r1 vs vo 2k

c1 vo gnd 2uF

.tran 0.01ms 1ms

.option post

.end

* Now save this file into a folder called “Sample”. Name it sample.sp.
* Then open the “HSPICE UI” (HSPUI for short) tool which is a graphical user interface to HSPICE. Whereas you can run HSPICE and CosmosScope separately, HPSPUI keeps HSPICE tool, CosmosScope tool, netlist, and the HSPICE simulation output (the .lis file described earlier) in a convenient panel for easy execution.
* Press Open and select sample.sp using the file browser. You will notice that HSPUI automatically takes the title and takes an output file called sample.lis, which is also available in the Sample directory.
* Click Simulate to execute the circuit. HSPUI will open HSPICE window for you and execute your netlist through HSPICE tool, generating sample.lis and other output files utilized by CosmosScope.
* Now click Edit LL option to observe the output from HSPICE simulation. This file includes information about the analysis performed by HSPICE. Usually, we look here for measurement results, operating points, and error messages.
* Click CosmosScope to run CosmosScope. You will observe that HSPUI opens your circuit simulations in CosmosScope, and you can now begin plotting of data.

**5.3 CosmosScope**

This section defines how to use CosmosScope tool to take measurements.

* Select File > Open > Plotfiles... to open a plotfile window that includes the signal(s) you desire to measure. The Signal Manager window opens, which includes all the signal data present at each node of circuit.
* Plot the signal waveform. You can either double-click on a signal or select a signal name and press the Plot button situated at the bottom of the Signal Manager window.
* Click the Measurement Tool button at the bottom of the main CosmosScope window to open the Measurement Tool window.
* In the Measurement Tool window, click the Measurement button, and select one of the available measurements.
* In the Active graph text box, select the graph that includes the signal you want to measure.
* Change any required parameters in the Measurement Tool window to generate the required measurement result.
* Then click Apply button to make the measurement.

**5.4 Technology Nodes**

The technology nodes such as 180 nm, 130 nm, 90 nm, 65 nm etc. played a very important role in the device performance. With the advancement in time scaling of the device technology node took place rapidly which lead to better device functions. The 32 nanometer (32 nm) node is another level following the 45 nm process in CMOS semiconductor device fabrication. 32 nm relates to the average half-pitch of a memory cell at this technology level. Enduring the Moore’s law to the 32 nm technology node needs difficult trade-offs in the source/drain contact area, the gate length and contact to gate margin. Due to reduction in dimensions, less source/drain contact area is available resulting in potential Rext increase and also less area for introducing strain for mobility increase to improve device performance.

The decrease in the source/drain area needs further enhancement in strain and contact technologies for mobility improvement and Rext reduction. The 32 nm technology utilizes fourth generation strained silicon and second generation high-k and replacement metal gate flow. The use of the replacement metal gate flow makes the stress enhancement technique able to be in place before removing the poly gate from the transistor.

NMOS saturation current Idsat increases by 19% and linear current Idlin increases by 20% in case of the 45 nm technology. The 32 nm transistor continues the historic trend of increased drive current while reducing gate pitch. These drive currents are the highest reported currents at the smallest gate pitch of any 32 nm or 28 nm technology.

**Chapter 6**

**PROPOSED WORK**

**6.1 4T SRAM Cell Design**

The most widely recognized SRAM cell comprises four NMOS transistors in addition to two poly-load resistors. Such configuration is known as 4T cell SRAM. Two NMOS transistors are the pass-transistors. Such transistors have their gates tied to the word line and then associate a cell to the columns. The two different NMOS transistors are force downs of flip-flop inverters. The inverter load comprises a high polysilicon resistor. This configuration is the most prevalent in light of its size contrasted with a 6T cell. The cell needs the room just for the four NMOS transistors. The poly loads are then stacked over these transistors. Despite the fact that the 4T SRAM cell might be smaller than the 6T cell, it is still around four times as extensive as the cell of comparable DRAM cell generation.

The complex nature of the 4T cell is to make the resistor load sufficiently high (in the scope of giga-ohms) to reduce the current. Though, this resistor must not be too high to ensure great usefulness. Regardless of its leverage size, the 4T cells have a few restrictions. It incorporates the way that every cell has current streaming in one resistor (that is, SRAM has high standby current), the cell is delicate to noise and soft error due to high resistance. Fig. 6.1 represents design of 4T SRAM cell. This design is simulated in HSpice tool using 45 nm and 130 nm CMOS technology.

Fig. 6.1 Labeled diagram of 4T SRAM cell

Table 6.1 Transistor’s characteristics for 4T SRAM

|  |  |
| --- | --- |
| **MOSFET** | **W/L ratio** |
| M1 | 1.54 |
| M2 | 1.54 |
| M3 | 1.92 |
| M4 | 1.92 |

**6.1.1 4T SRAM Read Mode**

When wordline (WL) is high, let Q = 1 and Qbar = 0. BL & BLbar act as output lines and are precharged. Voltage at Q and BL are same so no discharging occurs. Voltage at Qbar and BLbar are different so discharging occurs and BLbar voltage decreases that means Q =1.

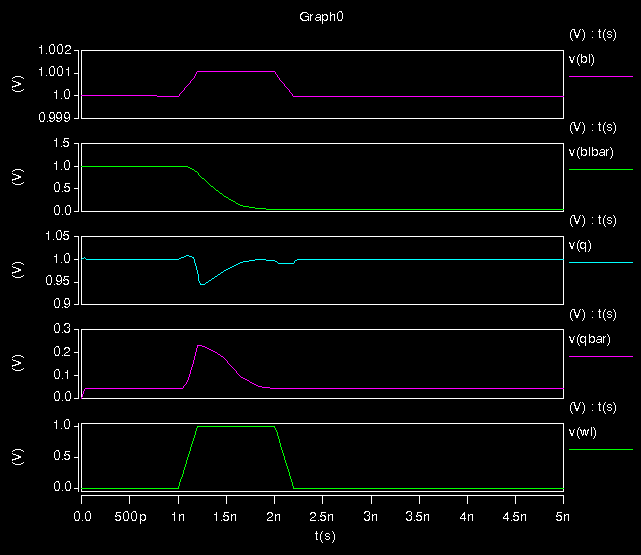
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Fig. 6.2 Waveforms for read mode of 4T SRAM cell

**6.1.2 4T SRAM Write Mode**

When wordline (WL) is high, let Q = 1 and Qbar = 0. We wish to write ‘0’ in cell. BL & BLbar act as input lines. Voltage at BL is grounded. Now Voltage at Q and BL are different so discharging occurs and Q = 0 due to ON state of M3. Voltage at Qbar and BLbar are different so discharging occurs and Qbar = 1 due to ON state of M4.

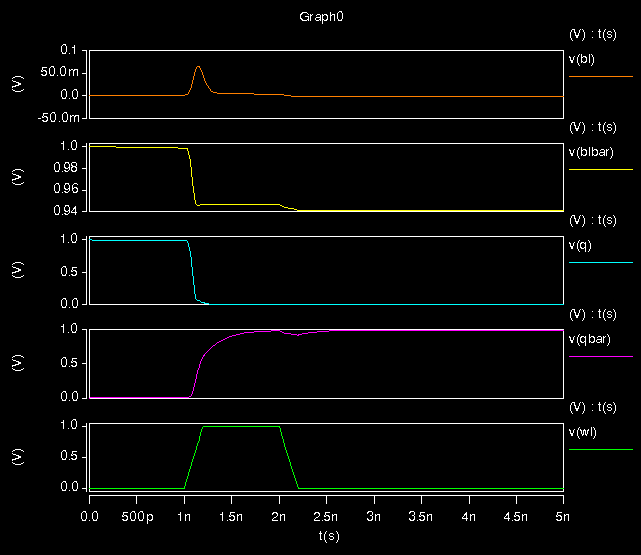
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Fig. 6.3 Waveforms for write mode of 4T SRAM cell

**6.2 Performance Parameter for Different Resistance and Capacitance**

Table 6.2 Performance parameter for SRAM cell in read mode at 130nm

|  |  |  |  |
| --- | --- | --- | --- |
| **S. No.** | **Resistor R1 & R2 (KΩ)** | **Capacitor C1 & C2 (pF)** | **Average Power (µW)** |
| 1 | 300 | 0.015 | 4.87 |
| 2 | 350 | 0.015 | 4.40 |
| 3 | 400 | 0.015 | 4.05 |
| 4 | 450 | 0.015 | 3.77 |
| 5 | 500 | 0.015 | 3.55 |
| 6 | 300 | 0.012 | 4.55 |
| 7 | 300 | 0.009 | 4.23 |
| 8 | 300 | 0.006 | 3.96 |
| 9 | 300 | 0.003 | 3.67 |

Table 6.3 Performance parameter for SRAM cell in write mode at 130nm

|  |  |  |  |
| --- | --- | --- | --- |
| **S. No.** | **Resistor R1 & R2 (KΩ)** | **Capacitor C1 & C2 (pF)** | **Average Power (µW)** |
| 1 | 300 | 0.015 | 3.73 |
| 2 | 350 | 0.015 | 3.28 |
| 3 | 400 | 0.015 | 2.90 |
| 4 | 450 | 0.015 | 2.62 |
| 5 | 500 | 0.015 | 2.41 |
| 6 | 300 | 0.012 | 3.76 |
| 7 | 300 | 0.009 | 3.79 |
| 8 | 300 | 0.006 | 3.83 |
| 9 | 300 | 0.003 | 3.92 |

Table 6.4 Performance parameter for SRAM cell in read mode at 45nm

|  |  |  |  |
| --- | --- | --- | --- |
| **S. No.** | **Resistor R1 & R2 (KΩ)** | **Capacitor C1 & C2 (pF)** | **Average Power (µW)** |
| 1 | 300 | 0.015 | 4.86 |
| 2 | 350 | 0.015 | 4.39 |
| 3 | 400 | 0.015 | 4.03 |
| 4 | 450 | 0.015 | 3.75 |
| 5 | 500 | 0.015 | 3.53 |
| 6 | 300 | 0.012 | 4.59 |
| 7 | 300 | 0.009 | 4.29 |
| 8 | 300 | 0.006 | 4.02 |
| 9 | 300 | 0.003 | 3.69 |

Table 6.5 Performance parameter for SRAM cell in write mode at 45nm

|  |  |  |  |
| --- | --- | --- | --- |
| **S. No.** | **Resistor R1 & R2 (KΩ)** | **Capacitor C1 & C2 (pF)** | **Average Power (µW)** |
| 1 | 300 | 0.015 | 3.58 |
| 2 | 350 | 0.015 | 3.11 |
| 3 | 400 | 0.015 | 2.77 |
| 4 | 450 | 0.015 | 2.52 |
| 5 | 500 | 0.015 | 2.32 |
| 6 | 300 | 0.012 | 3.61 |
| 7 | 300 | 0.009 | 3.67 |
| 8 | 300 | 0.006 | 3.76 |
| 9 | 300 | 0.003 | 3.89 |

Graphical representation of resistance versus average power and capacitance versus average power for results at 130nm and 45nm is shown below:

Fig. 6.4 Resistance versus average power at 130nm

Fig. 6.5 Capacitance versus average power at 130nm

Fig. 6.6 Resistance versus average power at 45nm

Fig. 6.7 Capacitance versus average power at 45nm

**6.3 Comparison with Previous Literature**

Table 6.6 Comparison of results with previous literature

|  |  |  |
| --- | --- | --- |
| **Reference** | **Average Power (µW)** | |
| **Read Mode** | **Write Mode** |
| Ref [39] | 20.00 | 15.45 |
| Proposed Design (130nm) | 4.87 | 3.73 |
| Proposed Design (45nm) | 4.86 | 3.58 |

**Chapter 7**

**CONCLUSION**

In this thesis, we have proposed the efficient design of SRAM cell which consists of 4 NMOS transistors and 2 resistors. Proposed 4T SRAM cell can reduce the power consumption and area of the SRAM. We have analyzed 4T SRAM cell using 45nm and 130nm CMOS technology.

Optimized value of resistance and capacitance for the efficient working of SRAM cell based on 45nm CMOS technology is 300KΩ and 0.015pF. At this value power consumed in read mode is 4.86 µW and in write mode is 3.58 µW.

Optimized value of resistance and capacitance for the efficient working of SRAM cell based on 130nm CMOS technology is 300KΩ and 0.015pF. At this value power consumed in read mode is 4.87 µW and in write mode is 3.73 µW.

Simulated results are compared with the previous results and found out that in read and write mode proposed 4T SRAM cell design consumes very less power when simulated in HSpice tool using 45nm CMOS technology. Therefore, it is concluded that our design shows better results. All the designs are simulated in HSpice tool using 45nm and 130 nm CMOS technology.

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